Bruno GHYSELEN holds a PhD in Materials science obtained in 1992 from University Paris 7. This work was on Josephson junctions and has been realised within THOMSON-CSF/ Laboratoire Central de Recherches /Orsay France (now within THALES).

He pursued this collaborative work by joining as a research associate the University of Cambridge (UK/ Materials Science Department). He then joined SOITEC mid 1995, just before SOITEC revealed its new Smart Cut ä technology dedicated to the manufacturing of a new generation of SOI substrates.

Within SOITEC, he has been in charge of different R&D programs and collaborations with different partners (silicon wafer suppliers, SOITEC customers, equipment suppliers, Universities, R&D public organizations ..).

Most of these programs were dedicated to the development of advanced SOI and other advanced composite substrates for specific applications. He has been involved in the development of ultra-thin or at the other extreme ultra-thick SOI substrates, high resistivity SOI for CMOS RF, high mobility SOI (strained silicon, multiple crystalline orientation, GeOI ..), SiC/GaN on Insulator, double SOI, IIIV materials composite substrates ... .